

TRANSPORTATION

College buses are available from different parts of the city. Also local / Volvo bus are plying between Ernakulam and varikoli.

PROGRAMME COMMITTEE

Patrons

Mr. M G George Muthoot
Mr. George Alexander Muthoot
Mr. George Varghese P

Advisory Committee

Dr. A C Mathai
Dr. S Pushpa kumar
Mr. K T Subramanian

Organizing committee

Dr. Reshmi N G
Mr. Girish Balakrishan
Mrs. Jisha James
Mrs. Divya Madhu
Mr. Mahalingam P R
Mr. Anand Hareendran S
Mrs. Sreenu G
Mrs. Jency Thomas

Important Dates

Last Date Of Registration : 22nd June 2016

Chief Co-Ordinator: Dr. Sanju V

ADDRESS FOR CORRESPONDENCE

Department Of Computer Science & Engg
Muthoot Institute Of Technology & Science
Varikoli, Cochin - 682308
(m) : 9448804710
email id : sanjuv@mgits.ac.in

WHO CAN REGISTER?

Persons from Industry and the Academia, The faculty members, interested researchers & post graduate students of multiple disciplines of engineering colleges (CSE / ECE / EEE / AEI / IT) are eligible to register for the workshop.

REGISTRATION FEES

Rs.1000/- for the Participants

ABOUT THE RESOURCE PERSONS

Resource persons are from Industry and Academia

ROUTEMAP



FACULTY DEVELOPMENT PROGRAM ON INTRODUCTION TO FPGA & ASIC DESIGN

June 27 – July 1, 2016

Organized by



Department of Computer Science and Engineering
Muthoot Institute Of Technology & Science
Varikoli P.O, Puthencruz- 682308
PH: 0484-2732111/100
www.mgits.ac.in

ABOUT THE COLLEGE

Muthoot Institute of Technology & Science (MITS) is promoted by Muthoot M. George Institute of Technology, a Section 25 Company within the Muthoot Group. MITS, a Self Financing Engineering College, situated in the Industrial suburb of KOCHI close to the Smart City and Info Park, nearly 15 kms from Vytilla Junction on the Kochi-Madurai National Highway. The College is approved by All India Council for Technical Education (AICTE) and affiliated to MG University. The current batch onwards, all Engineering colleges are affiliated to Kerala Technological University.

MISSION

To build a strong Centre of excellence for learning and research in engineering and technology, to facilitate students to learn and imbibe , along with their subjects of study, discipline ,ethics, tradition and culture, and to bring out students not only intellectually well-equipped but also combined with a value system which will enable them to become socially committed citizens.

VISION

- Moulding future leaders in technology by providing state of the art learning facilities and infrastructure.
- Engender in students the spirit of enquiry and entrepreneurship.
- Foster innovation and ideation on a sustained basis.
- Develop MITS into a Centre where direct linkage of education with industry experience is fostered.

SALIENT FEATURES

- Highly qualified faculty and other Technical Staff equipped with years of experience in identifying the potential of each student and turning into young engineers of Global standards.
- Provide scholarship to all Meritorious Students.
- Instructions based on Academic Planning
- Continuous evaluation programs
- Deficiency clearing tutorials
- Live Projects and assignments
- Career based programs
- Language reinforcement
- Well stocked Library and internet facility
- Well-equipped and spacious laboratories and workshops
- Continued improvement programs
- Strong industrial binding
- Experts in counseling Yoga, Meditation, and Communicative English will impact training in the respective fields aiming at the mental and spiritual development of the students.
- Placement opportunities for eligible students in the group companies in various Business verticals of Muthoot group.
- Hostel facility within the Campus, for both Men & Lady Students.
- College Bus facility is available.
- ATM facility available.

TOPICS COVERED

1. What is FPGA
2. FPGA Design with Verilog / VHDL
3. ASIC Design Flow
4. Research Opportunities

Registration Form Faculty Development Program On Introduction To FPGA & ASIC Design

June 27 – July 1, 2016

Name:

Designation:

Address of the Institution:

Contact Number:

Email id:

Signature:

Principal / HOD's Signature with seal